REMARKS

Claims 1-4 and 6-44 were presented for examination. Of these, claims 26-42 have been withdrawn from consideration. In the Office Action of June 17, 2004, claims 1-4, 6-25, 43 and 44 have been rejected. No claims have been allowed. Applicant respectfully requests reconsideration.

Under the heading "Specification," the Office Action requires a new title. The specification has been amended to adopt the title suggested by the Examiner.

Objections were made to the *claims* in the same section. Putting aside that there should have been a separate heading for this section of the Office Action, claims 15, 19-22 and 25 have been amended as suggested by the Examiner. Such amendments are not intended to change the scope of the claims.

Applicant will address the remainder of the Office Action using the headings therein, and in the same order as presented.

Double Patenting Rejection

All claims have been rejected for obviousness-type double patenting over claims 1-34 of U.S. Patent No. 6,462,977 to Butz. According to the Office Action, the claims are not patentably distinct from each other "because they both claim a substantially similar device comprising 'virtual columns' and 'addressing layers'." Applicant respectfully disagrees and requests reconsideration.

Taking, for example, claim 1 herein, such claim requires *inter alia* "a switching signal applied to an addressing layer is transmitted to all of the addressable switch elements within the addressing layer" and further requires "a plurality of serial connections of addressable switch elements, each serial connection including one switch element from each of the plurality of addressing layers, each serial connection separately located to establish a unique array address."

Independent claim 6 requires a system that includes a plurality of uniquely addressable locations comprising *inter alia*, "a plurality of virtual columns, each virtual column including a plurality of serially connected switch elements" and "serially connected switch elements of each virtual column are arranged such that a unique address for each virtual column is established."

Claim 10 requires a plurality of virtual columns, each including a plurality of addressable switch elements, and at least one addressing layer coupled to at least one of the plurality of addressable switch elements.

Claim 16 is drawn to a matrix of uniquely addressable locations, such matrix having a first virtual column including a first addressable switch element and a second addressable switch element, and a second virtual column including a third addressable switch element and a fourth addressable switch element.

Independent claim 26 is also drawn to a matrix of uniquely addressable locations. It comprises two or more addressing multi-layers, the addressing multi-layers including two or more sub-layers for conducting an addressing signal, and a plurality of virtual columns. The virtual columns include a plurality of addressable switch elements coupled to the two or more of the addressing multi-layers.

Claim 30 is drawn to a matrix of discretely addressable locations comprising an optically conductive material, a plurality of virtual columns wherein each includes at least two addressable switch elements and the columns are disposed in the optically conductive material; and a first signal generator that generates at least two different optical signals, at least one optical signal passing through the optically conductive material.

Claim 36 is also drawn to a matrix of uniquely addressable locations. In the case of this claim, the matrix comprises a plurality of addressing layers having a first portion of a first type and a second portion of a second type, the first portion allowing a signal to pass therethrough only upon receipt of a first signal type and the second portion allowing a signal to pass therethrough only upon receipt of a second signal type. At least two of the plurality of addressing layers are disposed such that an ordered alignment of the first and second portions of at least two of the addressing layers is established.

None of these claims is obvious over the claims of the '977 Butz patent. The mere fact that both sets of claims refer at times to virtual columns and addressing layers is not proof and does not suffice to establish that the claims herein are subject to an obviousness-type double patenting rejection. Note that claim 1 of the '977 patent is drawn to a data storage device; claim 22 is drawn to a device for storing data; claim 35 is directed to a data storage device; the same is true of claim 39; claim 40 is drawn to a memory device; claim 56 is directed to a memory device; and claim 57 relates to a method of accessing data in a data storage device. That is, all of

the claims of the '977 patent relate to memory. By contrast, the independent claims herein relate more broadly to addressing unique locations in an array (which may not include any memory) .

In view of the foregoing, withdrawal of the obviousness-type double patenting rejection is requested.

Rejections under 35 U.S.C. §112

The Examiner rejected claims 1-4, 6-25 and 43-44 under 35 U.S.C. §112, second paragraph as being indefinite. According to the Office Action, "numerous" claims recite indefinite terms because it is unclear what are meant by said terms. "Examples" of said terms are given. In fact, precisely and only three examples are given and it is only those three examples that can be addressed herein: "addressing layers" in claim 1, line3; "addressable switch elements" in claim 1, lines 3-4 and "virtual columns" in claim 6, line 3. If the Examiner has other terms in mind, the Examiner must identify them.

Applicant traverses this rejection.

There is nothing indefinite about the terms that have been identified as examples. Indeed, the same Examiner, in examining the application that became '977 patent, accepted these terms as definite! One skilled in the art certainly will understand them in light of the specification. No reason has been cited that they are indefinite, merely a conclusion. That is an improper basis for rejection. The burden is on the Examiner to support the rejection with facts. Moreover, the Examiner is directed to the following portions of the specification and drawings which explain and define the identified terms clearly and unambiguously:

A. "Addressing Layer"

Regarding "addressing layer" - page 6, lines 25-26, indicating that "Fig. 3 is a diagram of two virtual columns connected to a plurality of addressing layers;" page 6, lines 29-30, indicating "Fig. 5 is a cut-away view of a virtual column disposed through an addressing layer and an insulating layer;" page 7, lines 6-7, indicate "Fig. 8 is an exploded view of two addressing layers showing an example of how addressing layers of some embodiments of the present invention may be constructed;" page 8, lines 7-10, state "Fig. 20 shows a plurality of virtual columns passing through addressing layers which are constructed such that the addressable switch element performs a column disabling as opposed to a column enabling function when the appropriate signal is applied thereto."

Page 11, lines 23-27 notes that in one embodiment switch elements 304 and 304′ may receive a signal from a first addressing layer 310.

On page 12, from lines 10-15, the application explains that each addressable element is enabled only when it receives the appropriate input signal value and then states "Thus, if the first signal "value" or "type" is presented on all three addressing layers, 310, 312, and 314, then all of the addressable switch elements of the first virtual column 300 are enabled and the first virtual column 300 becomes active."

Turning to another example, the specification explains on page 13, at lines 13-15, "the addressable switch elements 408 are coupled to addressing layers 410 capable of transmitting signals to the addressable switch elements 408."

On page 13, line 28 - page 14, line 25, the nature of the addressing layers as signal conducting layers (whether electrical or optical) is made abundantly clear:

> "In this example, the addressing layers 410 are separated from adjacent addressing layers by insulating layers 412. These insulating layers 412 serve to keep any signal present on one addressing layer from interfering with a signal on another addressing layer. Of course, the insulating layers are not necessary if the signals being received do not interfere with one another. For example, if the signals are light signals, the insulating layers may not be needed.
>
> Each addressing layer 410 may be adjacent to and conduct a signal to one of the addressable switch elements 408 of each of the virtual columns 404 disposed in the matrix 400. Each addressing layer 410 may be formed from any material which may carry a signal. For instance, the addressing layers 410 may be formed from an electrical conductor such as gold, silver, copper, aluminum foil, aluminum film material, and the like if the addressable switch elements 408 respond to electrical input signals. Alternatively, the addressing layers 410 may be formed from a photo-conductor which transmits light such as glass or a polymer if the addressable switch elements 408 respond to optical input signals. In one embodiment, each addressable switch element 408 of the virtual columns 404 may be surrounded by a conductive material and if a plurality of virtual columns 404 are brought into contact with one another, conductive material portions surrounding the addressable switch elements 408 may contact one another and thereby form a conductive addressing layer.

> In general, the matrix 400 of this embodiment works as follows. An external device, such as a central processing unit (CPU) of a computer or other suitable controller 422, alerts the matrix 400 that the device needs to access, store information or send information to a particular location in or to the matrix 400. This may be accomplished in a variety of ways. For instance, the matrix 400 may have an enable line (not shown) connected to the external device which enables the matrix 400 upon receipt of a signal on the enable line. Alternatively, the matrix 400 may be directly connected to the external device in a "master-slave" arrangement and, in that case, no enabling signal is required.
> Regardless, after the matrix 400 is ready to conduct either reading or writing signals (i.e., it is enabled), an address is transferred to the addressing layers 410. The signal on each addressing layer is transferred to an addressable switch element 408 of each of the virtual columns 404."

Thus, there can be no doubt that the meaning of "addressing layer" is clear and express.

B. "Virtual Column"

"Virtual column" is also, contrary to the Office Action, quite clear. To cite just a few examples of where the term is explained, the Examiner is directed to page 8, lines 13-18. There, in the opening paragraph of the "Detailed Description", the specification recites:

> "Aspects and embodiments of the present invention are related to matrices of uniquely addressable locations. The matrices of embodiments of the present invention may include a plurality of virtual columns. As used herein, and described in greater detail below, a virtual column is a construct that includes a plurality of addressable switch elements (or "switch elements") that are used to uniquely address each virtual column."

Further, from page 9, line 27-page 10, line 6, the application explains:

> "According to one embodiment, each addressable switch element is responsive to only one of two possible signal types. When the signal to which the particular element is responsive is received by the addressable switch element, the addressable switch element becomes "active" or "conductive" and allows a signal to pass through its signal transmission channel (as opposed to its switching channel) in a ("perpendicular") signal pathway separate from the addressing or activation pathways. If all of the addressable switch elements of the virtual column have received, and continue to receive, the signal that activates them, the virtual column 200 becomes conductive. When the virtual column 200 becomes conductive, signals may pass through it. In data storage

> embodiments, when the virtual column 200 is conductive, the information contained in the data storage element 201 may be accessed. The read out layer 210 may be used, as discussed below, to both read information out of the storage element 201 as well to play a part in storing information in the storage element 201.

Thus, the term "virtual column" is preferably clear. Fig. 2 shows one example of a virtual column, including two addressable switch elements. The specification makes clear that a virtual column may contain any number of addressable switch elements and may or may not also include a data storage element.

Any rejection based on indefiniteness of the term "virtual column" is thus unfounded.

C. "Addressable Switch Element"

"Addressable switch element" is understandable on its face. A switch or switch element is one of the most basic building blocks of electrical and computational circuitry. Addressing of elements in a matrix, memory, etc., is another basic construct of electrical engineering and computer science. One skilled in the art of electrical engineering or computer science would readily appreciate the term "addressable switch element." The operation of such a device is expounded at various places in the specification and drawings, including at page 9, line 27-page 10, line 6:

> "According to one embodiment, each addressable switch element is responsive to only one of two possible signal types. When the signal to which the particular element is responsive is received by the addressable switch element, the addressable switch element becomes "active" or "conductive" and allows a signal to pass through its signal transmission channel (as opposed to its switching channel) in a ("perpendicular") signal pathway separate from the addressing or activation pathways. If all of the addressable switch elements of the virtual column have received, and continue to receive, the signal that activates them, the virtual column 200 becomes conductive. When the virtual column 200 becomes conductive, signals may pass through it. In data storage embodiments, when the virtual column 200 is conductive, the information contained in the data storage element 201 may be accessed. The read out layer 210 may be used, as discussed below, to both read information out of the storage element 201 as well to play a part in storing information in the storage element 201."

Further, at page 10, lines 11-17, it is stated as follows:

> "In this example, the addressable switch elements 202 and 204 may be electrical switches such as transistors which allow a current to pass there-through when receiving the required input signal and the feed-through 208 may be any conductor implemented as an electrical connection between the transistors (e.g., a wire). In other embodiments, the addressable switch elements 202 and 204 may be optical switches that allow energy (e.g., light or electrical energy) to pass through them when activated, and the feed-throughs may be optical fibers."

In other words, Applicant has used the three terms identified by the Examiner as generic terms not requiring implementation as electrical devices or optical devices, allowing the invention to be explained at a level of abstraction that permits both kinds of implementations. The terms, and their use, are more than sufficiently definite for those skilled in the art to understand how to make and use the invention. That they include various implementations in no way makes them indefinite. Reconsideration and withdrawal of the rejection is requested.

Claims 16-25 next are rejected under 35 U.S.C. §112, second paragraph, as being "incomplete for omitting essential structural cooperative relationships of elements, such omission amounts to a gap between the necessary structural connections." Specifically, the Office Action states that there is an omitted structural cooperative relationship between the first virtual column, second virtual column and either each other or other claimed elements. The Examiner's point is noted. In response, claim 16 has been amended to recite an addressing layer coupled to at least one of the adjustable switch elements of the first virtual column and to at least one of the addressable switch elements of the second virtual column. A conforming amendment has been made to claim 17, though the scope of claim 17 will be seen not to have changed.

Claim Rejections under 35 U.S.C. §102

All claims have been rejected as anticipated by Fellows. Unfortunately, however, the Examiner has provided no reading of Fellows against any of claims 1-4, 6-13, 16-23 or 43-44. On its face, therefore, the rejection can not stand. It literally begs Applicant to try to get inside the Examiner's mind to figure out why the Examiner believes such claims are anticipated. Applicant is not required to be a mind reader. The Examiner has to explain, limitation-by-limitation, how he finds anticipation.

To further the prosecution of the application, but without relieving the Office of the burden of substantiating its rejections, and in the hope of advancing prosecution toward allowance, Applicant states the following:

Fellows discloses a fiber optic computational network which is constructed from fiber optic gate computing elements. A gate computing element includes a fiber optic housing that holds a number of optical cells, which are composed of non-linear organic polymers (Abstract). The optical cells can be combined and operating in such a manner as to achieve Boolean AND and OR gate computing elements (col. 1, lines 17-22).

As illustrated in Fellows' figure 1, a dual-channel gate computing element may consist of three optical cells 20-21 and 22 (col. 3, lines 23-27). The optical cells are confined within the fiber optic 32 (col. 3, lines 55-56). Each cell 20, 21, and 22 is composed of two non-linear organic polymers. For instance, optical cell 20 contains the two non-linear organic polymers 2 and 5. Each non-linear organic polymer is contacted by a piezoelectric crystal half-ring, such as half-ring 8, which contacts non-linear organic polymer 2 (col. 3, lines 50-52). A photovoltaic device 15 controls each piezoelectric crystal half-ring (col. 3, line 51-col. 4, line1). Optical input signals may be provided for the right channel at A_1, A_2, A_3, and for the left channel at B_1, B_1,B_2, B_3, and are received by respective photovoltaic devices 15a-15f (col. 3, lines 61-65). An output detector 43 may be positioned to receive light from the incident laser 10 that has been transmitted through all three optical cells 20-22 (col. 4, lines 38-45).

In operation, an optical input signal at A_1 induces photovoltaic device 15a to generate a voltage. The generated voltage creates a voltage potential on the piezoelectric crystal half-ring 8, which will then transmit an acoustic stress wave through the non-linear organic polymer 2. The acoustic stress wave results in a change in the index of refraction of non-linear organic polymer 2, such that a portion of the incident laser 10 is able to be transmitted through the non-linear organic polymer 2 (col. 4, lines 11-28). Similarly, an optical signal detected at the input B_1 will result in a portion of the incident laser 10 being transmitted through the non-linear organic polymer 5. Analogous behavior is exhibited for optical cells 21 and 22. Therefore, by connecting photovoltaic devices 15a and 15b with a conduction path or cable 25, an input at A_1 **or** A_2 will induces both photovoltaic devices 15a and 15b to create a voltage, leading to a change in the index of refraction of organic polymers 2 **and** 3. Thus, by using conduction paths to

connect the photovoltaic devices 15a-15f in appropriate combinations, the optical gate of Fig. 1 may perform the AND or OR operation (col. 4, line 46-col. 5, line 7 and lines 37-66).

Fig. 6 of Fellows shows an embodiment in which a gate element includes more than three optical cells, and each optical cell includes eight non-linear organic polymers. The operation of the gate element is analogous to that just described for the gate element of Fig. 1. Fig. 7 shows a combination of optical gates between elements performing a computational network.

Claim 1 is directed to a system for addressing unique locations in an array. The system comprises, *inter alia*, a plurality of addressing layers, each addressing layer including addressable switch elements of at least two types, each type of switch element being responsive to at least one of at least two types of switching signals. Claim 1 further requires that a switching signal applied to an addressing layer be transmitted to all of the addressable switch elements within the addressing layer.

Fellows clearly does not teach the limitations of claim 1. The description of Fellows states "It can be seen therefore that FIG. 1 shows three segments or **layers** in this dual channel optical gate design, each essentially representing one gate input stage that transmits output to the next gate stage or segment." (col. 4, lines 46-50) [Emphasis added.] *However, those "layers" are in no way comparable to the addressing layers of claim 1.* The "layers" of Fellows do not include addressable switch elements of at least two types, each type of switch element being responsive to at least one of at least two types of switching signals. Additionally, Fellows does not disclose that a signal applied to a "layer" is transmitted to all of the addressable switch elements within the addressing layer.

However, with the benefit of hindsight provided by Applicant's disclosure, one may inappropriately attempt to construe the channels of Fellows as "addressing layers". Fig. 2 of Fellows discloses a dedicated optical OR gate (col. 5, lines 67-col. 6-line 5). A conduction path 25 is placed between the inputs A_1, A_2, and A_3, and similarly between inputs B_1, B_2, and B_3. Thus, an optical input signal applied to any of A_1, A_2 , or A_3, will effectively be transmitted to all of the non-linear organic polymers 2, 3, and 4, which form the right channel. Similarly, an optical input signal applied to any of B_1, B_2, or B_3 will effectively be transmitted to all of the non-linear organic polymers 5, 6, and 7, which form the left channel. One might be tempted to characterize the device as containing two addressing layers, the first "addressing layer"

corresponding to the right channel, and the second "addressing layer" corresponding to the left channel. This would be an improper interpretation of Fellows. Claim 1 requires that each addressing layer includes addressable switch elements of at least two respective types, each type of switch element being responsive to at least one of at least two types of switching signals. This limitation is not met by the channels of Fellows. In summary, Fellows does not teach the addressing layers of claim 1.

Claim 1 is thus novel over Fellows for at least these reasons.

Similar comments can be offered with respect to the other independent claims. However, inasmuch as the Examiner has not given a *prima facie* basis for the rejection, Applicant will withhold for the moment further distinguishing Fellows from each of the other independent claims. The distinctions actually should be obvious at this point.

The section 102 rejection thus should be withdrawn in its entirety. If the Examiner is not now persuaded to that effect, then at least a new, non-final action should be issued wherein the Examiner articulates more clearly the basis for the section 102 rejection, explaining how he finds each of the limitations of each of the rejected claims in the reference.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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